研究主題：積層三維積體電路與類神經運算技術

Biography:

Prof. Yeh has been dedicated to this research field of two-dimensional (2D) electronics and nanotechnology for a long time. He was granted a PhD degree in the Institute of Electronics Engineering by National Tsing Hua University (NTHU) for his work on high-speed 2D electronics and ferromagnetic oxide materials. Subsequently, he worked as a postdoctoral researcher in the same research group under the supervision of Prof. Po-Wen Chiu to develop **scalable 2D transistors and integrated circuits** leveraging CVD methodology for various 2D semiconductor growth. Following his research journey at NTHU, he joined Prof. Kaustav Banerjee's group in the Electrical and Computer Engineering Department at the University of California, Santa Barbara, from 2019-2022. Since then, he's been digging into 2D **Nanotransistors, non-volatile 2D resistive random-access memory (NV 2D-RRAM)**, and **monolithic 3D-ICs technology**, and he has been dedicated to the field of 2D electronics for over 15 years. Noteworthily, his first-author's research works accepted at 2020 International Electron Devices Meeting (**IEDM**), the world's most renowned flagship conference in the areas of semiconductor and electronic device technology, is the invention of 0.5T0.5R memory cell with h-BN switching layers has been highlighted by one of the most prestigious journal, "Nature Electronics" since this smallest footprint among all reported layered-material based memory units with transistor is the first-ever demonstration in 2D RRAM technology history.

It is noted that Prof. Yeh is an expert with extraordinary ability in the field of semiconductor engineering and material science, who has sustained national and international acclaim and authored/co-authored over 50 referred articles. His contributions have been recognized and published in renowned venues, including ***ACS Nano*** (IF:15.88), ***Nature Communications*** (IF: 14.919), ***Nano Letters*** (IF: 11.19), ***Advanced Materials*** (IF: **30.85**), **IEEE *Transactions on Electron Devices* (T-ED)**, etc., where Prof. Yeh has his *total citation* and *h-index* reaching up to 4489+ and 29, respectively. It is noted that Prof. Yeh has had his first-author's paper up to 5 out of 14 publications in **ACS Nano**. (***ACS Nano*** is the world-renowned journal showing the "**Top 1**" in worldwide h5-index ranking in the field of Nanotechnology.) On the other hand, he has been inventor/co-inventor of **10** patents associated with 2D materials synthesis and fabrication apparatuses. In his first two years at NTHU, Prof. Yeh achieved the prestigious honors of **Yushan Young Fellows** (**2022-2027**) and **ASPEED**

Young Fellows (**2022 & 2023**) and received **NTHU EECS Research Awards for Newly Recruited Faculties** (2024), all of which stand as strong evidence of his dedication and proficiency in his research field.

Prof. Yeh's primary research expertise lies in developing 2D electronics and using various growth techniques (CVD and MOCVD) to synthesize 2D semiconductors and heterostructures for **monolithic 3D integration technology**. He is skilled in fundamental device physics and characterization of 2D material systems. Recently, his significant contributions include the improved layered thin-film deposition at low-temperature (< 500 ℃), high-performance integrable 2D nanotransistors, **a new approach of energy-efficient neuromorphic architectures, and state-of-the-art CFET with monolithic hetero-integration leveraging 2D materials**, have brought great benefits to new-generation computing technology.

葉教授在二維電子學和奈米技術領域擁有超過 15 年的研究經驗，於國立清華大學取得博士學位，專攻高速二維電晶體與鐵磁氧化物材料。其後，他在邱博文教授指導下進行博士後研究，專注於二維材料積體電路的開發。2019 年至 2022 年，葉博士加入加州大學聖塔芭芭拉分校 Kaustav Banerjee 教授團隊，**深入研究二維奈米電晶體、非揮發性二維阻變記憶體（NV 2D-RRAM）及三維積體電路（3D-ICs）**技術。

葉教授於 2020 年國際電子元件會議（IEDM）上發表的研究成果，發明了世界上最小的基於層狀材料的 0.5T0.5R 記憶單元，這項突破性的技術被 Nature Electronics 高度評價。他已發表 50 篇經過同行評審的論文，總引用次數超過 4489 次，h 指數達 29，且為多項專利的發明/共同發明人。

葉教授曾獲玉山青年學者獎、信驊青年學者獎，以及清華大學新聘教師研究獎，顯示他在研究領域的卓越貢獻。葉教授的主要研究專長包括開發二維電子學，以及有機金屬氣相沉積技術合成二維半導體與異質結構，應用於先進晶片整合技術。同時他擅長二維材料系統的基本元件物理與設計。近期，他的重要貢獻包括在低溫（<500℃）下改良沉積技術，使高效能整合二維奈米電晶體，進一步完成**二維材料實現積層型先進異質 CFET 與類神經運硬體架構**等新技術，這些研究為新一代運算科技帶來巨大的突破與發展。